BALL GRID ARRAY WITH BUMPS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims benefit of U.S. Provisional Patent Application Serial Nos. 60/456,618, filed March 21, 2003, and 60/449,684, filed February 25, 2003, the disclosures of which are incorporated by reference herein.

BACKGROUND OF THE INVENTION

[0002] The present invention relates to microelectronic packaging and sockets.

[0003] Semiconductor chips are formed as a small, generally flat bodies with large and front rear surfaces and with contacts on the front surface electrically connected to electrical devices within the body. Although a semiconductor chip can be mounted directly to a circuit board, this requires special handling and mounting techniques. Therefore, chips are ordinarily provided as "packaged" units. A packaged chip includes the chip itself together with structures which at least partially cover surfaces or edges of the chip and which typically define terminals distinct from the contacts of the chip itself but electrically connected to such contacts. The packaged chip can be handled as a unit and can be mounted to external structures such as circuit boards using conventional techniques.

[0004] One form of packaged chips which has become increasingly popular is the "ball grid array" package. Such a package incorporates a chip carrier having a dielectric layer and terminals on the dielectric layer. The chip overlies a surface of the dielectric layer, with the front or back surface of the chip facing toward the dielectric layer. The terminals on the dielectric layer are connected by internal leads or wires of the package to the contacts on the chip. Typically, the terminals are formed as flat, disc-like elements integral with traces on the dielectric layer.

[0005] Such a package ordinarily is mounted on a circuit panel having contact pads exposed at a top surface by placing the package over the panel so that the terminals of the package are aligned with the contact pads on the package, with solder balls disposed between each terminal and the aligned contact pad. The solder balls are remelted or "reflowed" so as to form physical and electrical interconnections between the terminals and the contact pads. This type of mounting is compatible with the normal surface-mounting techniques used for mounting many components to circuit bumps. Ordinarily, the solder balls are prepositioned on the terminals of the packaged chip as part of the package manufacturing process, so that the entire unit can simply be placed on the circuit board with a flux if necessary and reflowed to complete the mounting process.

[0006] Although ball grid array packaging has been widely adopted, still further improvements would desirable. Typically, ball grid array packages are tested by engaging them with a test fixture having test contacts in a pattern corresponding to the pattern of contact pads on the circuit panel and applying signals and power to the chip through the solder balls and terminals. It is difficult to test ball grid array packages prior to mounting the solder balls on the contact pads. The solder balls project from the package and hence can be more readily engaged with a test fixture such as a socket. However, the solder tends to contaminate the test fixture as the test fixture is used repeatedly. Further, the solder typically used in a standard ball grid array package has a high lead content. There is increasing concern about this lead contaminating landfills and water supplies when the parts are disposed of. For these and other reasons, further enhancements would be desirable.

SUMMARY OF THE INVENTION

[0007] One aspect of the invention provides a chip carrier. A chip carrier according to this aspect of the invention desirably includes a dielectric layer having an inner surface facing upwardly and an outer surface facing downwardly, as well as conductive traces on the dielectric layer. The chip carrier according to this aspect of the invention desirably includes conductive bumps formed integrally with the traces. The conductive bumps project downwardly from the traces and have bottom ends which are adapted for bonding to contact pads on a circuit panel. As further discussed below, the integrally formed bumps and traces most preferably are formed from a single piece of metal, and the dielectric layer desirably is a coherent, self-supporting structure which can support and position the bumps and traces independently of any chip to which the carrier may subsequently be attached.

[0008] Most preferably, some or all of the bumps on the chip carrier are generally cup-shaped structures, preferably hollow, with a closed end of the cup shape defining the bottom end of the bump and an open end of the cup shape facing upwardly. Thus, the bumps desirably have a bottom wall portion defining the bottom end of the cup shape and first and second wall portions joining the bottom wall portion and extending upwardly therefrom, at least one of such wall portions joining one of the traces. Desirably, some or all of the bumps have exterior surfaces in the form of a surface of revolution about a generally vertical axis. The bumps desirably define lead-in surfaces sloping upwardly and outwardly around the entire periphery of the bump, adjacent the bottom end of the bump. In one arrangement, the traces are disposed on the inner side of the dielectric layer, and the bumps extend at least partially through the dielectric layer. The bumps may extend entirely through the dielectric

layer, so that the bottom ends of the bumps are disposed below the outer surface of the dielectric layer.

[0009] A further aspect of the invention provides a packaged chip which includes a chip having front and rear surfaces and contacts on the front surface, as well as a chip carrier which may include the features discussed above. The dielectric layer desirably extends beneath the chip, and the inner surface of the dielectric layer of the chip carrier faces upwardly toward the chip. Desirably, at least some of the bumps are disposed beneath the chip. The chip carrier may have leads formed integrally with the traces and bumps, such leads being bonded to contacts of the chip. Alternatively, the chip carrier may include bonding pads electrically connected to the traces and desirably formed integrally therewith, as well as bond wires formed separately from the traces and bonding pads, the bond wires connecting the bonding pads to the contacts. The packaged chip may include the chip in a face-down orientation, such that the front or contact-bearing surface of the chip faces toward the chip carrier, or in a face-up orientation, with the rear surface of the chip facing downwardly toward the chip carrier. The bottom ends of the bumps desirably are movable with respect to the chip. As further explained below, movability of the bump bottom ends may include some movability attributable to deformability of the bumps themselves. The packaged chip may further include a spacer layer disposed between the chip and the dielectric layer of the chip carrier. This spacer layer optionally may be a compliant structure which contributes to movability of the bump bottom ends.

[0010] Yet another aspect of the invention provides a microelectronic assembly which may include a packaged semiconductor chip, as discussed above, in conjunction with a circuit panel having a top surface and contact pads exposed at the top surface. The bottom ends of the bumps on the chip

carrier desirably are bonded to the contact pads on the circuit panel. As further discussed below, only a small amount of conductive bonding material need be used to join the bottom ends of the bumps to the contact pads of the circuit panel. For example, the conductive bonding material may include a thin film extending over a portion or all of the desirably convex bottom surfaces of the bumps and may form fillets extending from the contact pads to locations on the vertically-extensive wall surfaces of the bumps, above the bottom ends of the bumps. These fillets may extend entirely around each individual bump. Such a structure forms a strong joint with good resistance to stresses which may be imposed upon on it in service or in manufacture as, for example, stresses resulting from differential thermal expansion of the circuit panel and elements of the chip package such as the chip itself. In certain preferred embodiments, the bumps may provide flexibility similar to that imparted by solder balls having a height equivalent to that of the bumps. However, the assembly contains substantially less solder than an assembly including such large solder balls.

[0011] Yet another aspect of the invention provides methods of making microelectronic assemblies. The assembly methods according to this aspect of the invention may include a step of temporarily engaging a chip assembly such as those discussed above with a test fixture, so that the bottom ends of the bumps engage test contacts on the fixture, and testing the chip assembly by transmitting signals between at least some of the engaged bumps and test contacts. After testing, the assembly desirably is disengaged from the test fixture and mounted on a circuit panel by bonding the bottom ends of the bumps to contact pads on the circuit panel. During the temporary engagement step, the bottom ends of at least some of the bumps desirably are displaced vertically relative to the bottom ends of others of the bumps. Here again, the

displacement of the bump bottom ends may arise at least in part from deformation of the bumps themselves.

[0012] A still further aspect of the present invention provides methods of making chip carriers such as those discussed above. The methods of making the chip carriers desirably includes the step of uniting a metal with a dielectric layer having inner and outer surfaces, forming traces on the dielectric layer from the metal, and forming metallic bumps by deforming the metal. The uniting, bump-forming and trace-forming steps preferably are performed so that the bumps are integral with the traces and project downwardly from the traces. The bump-forming step may be performed after the step of uniting the metal with the dielectric layer as, for example, by deforming the metal through openings in the dielectric layer. The deforming step may be performed before or after the trace-forming step. Fabrication of the chip carrier may include other steps as, for example, forming leads integral with the traces and performing operations on the dielectric layer itself, such as forming bond windows. As discussed below, certain preferred methods according to this aspect of the invention can form chip carriers with bumps as discussed above at little or no additional cost over and above that incurred in forming otherwise comparable chip carriers having flat terminals.

[0013] As also described below, the bumps and chip carriers discussed herein can be used in other assemblies as, for example, to provide a socket in which the open ends of cup-shaped bumps serve as contacts for receiving other structures. In a socket according to yet another aspect of the invention, the bumps provide a "stand-off" supporting a dielectric element above a substrate and allow flexure of the dielectric element, so that another conductive element can be engaged with sockets mounted to the dielectric element, remote from the bumps themselves. Also, packaged chips as discussed

above can be stacked. In one such arrangement, the bumps incorporated in one packaged chip serve as sockets receiving the bumps of the next adjacent chip carrier.

[0014] These and other objects, features and advantages of the present invention will be more readily apparent from the detailed description of the preferred embodiments set forth below, taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] FIG. 1 is a diagrammatic top plan view depicting certain elements of a chip carrier during a process of forming the chip carrier.

[0016] FIG. 2 is a sectional view taking along line 2-2 in FIG. 1.

[0017] FIG. 3 is a view similar to FIG. 2, but depicting the elements at a later stage during the process.

[0018] FIG. 4 is a diagrammatic sectional view depicting a packaged chip incorporating the chip carrier of FIGS. 1-3.

[0019] FIG. 5 is a diagrammatic view depicting the packaged chip of FIG. 4 during one stage of a testing and assembling process.

[0020] FIG. 6 is a diagrammatic sectional view depicting a microelectronic assembly incorporating the packaged chip of FIGS. 4 and 5 in conjunction with a circuit panel.

[0021] FIG. 7 is a fragmentary view on an enlarged scale depicting a portion of the assembly shown in FIG. 6.

[0022] FIG. 8 is a diagrammatic sectional view similar to FIG. 6, but depicting an assembly in accordance with a further embodiment of the invention.

[0023] FIG. 9 is a diagrammatic sectional view depicting a packaged chip in accordance with a further embodiment of the invention.

[0024] FIG. 10 is a fragmentary, diagrammatic perspective view depicting certain portions of a chip carrier and assembly in accordance with a further embodiment of the invention.

[0025] FIG. 11 is a fragmentary, diagrammatic perspective view depicting portions an assembly in accordance with yet another embodiment of the invention.

[0026] FIG. 12 is a diagrammatic elevational view depicting an assembly in accordance with yet another embodiment of the invention.

[0027] FIG. 13 is a fragmentary, diagrammatic sectional view depicting portions of the assembly shown in FIG. 12.

[0028] FIG. 14 is diagrammatic sectional view depicting portions of a socket in accordance with a further embodiment of the invention.

[0029] FIGS. 15-18 are diagrammatic sectional views depicting portions of a chip carrier in accordance with a further embodiment of the invention during progressively later stages in manufacture of the chip carrier.

[0030] FIG. 19 is a diagrammatic sectional view depicting a portion of a chip carrier in accordance with one embodiment of the invention during a stage in a manufacturing process.

[0031] FIG. 20 is a diagrammatic sectional view depicting a portion of a chip carrier in accordance with yet another embodiment of the invention.

[0032] FIG. 21 is a fragmentary, diagrammatic sectional view depicting portions of yet another chip carrier in accordance with a further embodiment of the invention.

[0033] FIG. 22 is a fragmentary, diagrammatic sectional view depicting a portion of an assembly in accordance with a still further embodiment of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0034] A method of making a package according to one embodiment of the invention utilizes a substrate 20 incorporating a dielectric layer 22. Only a small portion of the dielectric layer is shown in plan view in FIG. 1. Layer 22 is generally planar plate-like or sheet-like structure having an inner side 24 seen in FIG. 1 and an oppositely

facing outer side 26 (FIG. 2). For example, layer 22 may be a circuit board formed from a conventional material such as FR4, FR5 or BT resin reinforced composite or a flexible circuit panel formed from a relatively thin layer of reinforced or unreinforced polymeric material such as, for example, polyimide. Layer 22 has bond windows 28 extending through the layer from the inner side to the outer side and also has bump openings 30 (FIG. 2) extending through it. Substrate 20 further includes a metallic layer 32 disposed on the inner surface 24 of dielectric layer 22. Metallic layer 32 incorporates a large number of lead units. Each such unit includes a lead 36 projecting across one of the bond windows 28; a trace 38 integral with the lead and extending across a portion of the inner surface and a bump-forming element 40 integral with the trace 38 and lead 36 disposed over one of the bump openings 30. The ends of leads 36 remote from the associated traces 38 are anchored to the dielectric layer by anchors 42 on the opposite side of the bond windows from the traces 38. Each anchor is connected to the associated lead by the relatively weak, frangible element 44 having tensile strength substantially smaller than tensile strength of lead 36. For example, each frangible element may be a section of smaller cross sectional area than the lead. In the particular arrangement illustrated, the bond windows are elongated, slot-like structures and numerous leads 36 project across each bond window. However, any arrangement of leads and bond windows can be employed. The structure of the leads and bond windows may be, for example, as shown in U.S. Patents 5,915,752 and 5,489,749.

[0035] The substrate in the condition illustrated in FIGS. 1 and 2 may be fabricated by conventional processes as, for example, by uniting a continuous layer of metal with a dielectric layer and selectively etching the metallic layer to form the lead units, or by uniting metal and dielectric by

depositing a metallic layer selectively onto the surface of the dielectric layer to form the lead units. The bond windows 28 and bump openings 30 may be formed by ablating, etching or mechanically punching the dielectric layer either before or after uniting the dielectric layer with the metallic layer. As mentioned above, only a small fragment of substrate is depicted in FIGS. 1 and 2. The substrate may be provided as a large, continuous tape or sheet suitable for forming numerous chip carriers to be associated with numerous chips, or can be provided as smaller units down to a substrate suitable for forming a chip carrier for a single chip.

[0036] In the next stage of the process, metallic layer 32 and particularly the bump-forming elements 40 are deformed by engaging the metallic layer with a punch 46 having projections 48 and moving the punch downwardly, in the direction indicated by arrow 50 in FIG. 3. The tips of the projections engage the bump-forming elements 40 of the metallic layer and deform those bump-forming elements into bumps 52 which are generally cup-shaped, hollow shells surrounding the tips of the projections. The bumps 52 extend downwardly through bump openings 30 so that the bumps 52 project beyond the lower or outer surface 26 of the dielectric layer.

[0037] Bumps 52 are formed integrally with traces 38. That is, a single metal forms at least a part of the trace and at least a part of the downwardly-extending bump, and this single metal extends into the bump and into the trace as a continuous body without a weld or joint. Either or both of the bump and the trace can include additional metals, which may be the same or different, and which may or may not be continuous with one another. The bumps can be formed from essentially any metal which has the desired conductive and bondability properties. Most commonly, the bumps and traces are formed from copper or a copper alloy, with or without a layer of gold or other oxidation-resistant, bondable metal. Such additional metals

can be applied by conventional plating processes. The bumps can be disposed side by side or in arrays with small spacings between adjacent bumps, as, for example, center-to-center distances less than about 1 mm. The bumps typically protrude from the outer surface of the dielectric by about 10 to about 150 microns.

[0038] In this condition, that portion of the substrate 20 forming each chip carrier, together with the traces 38, leads 36 and bumps 52 on such portion of the substrate, form a coherent, self-supporting structure. That is, the substrate supports the traces and bumps, and holds these elements at least substantially in position relative to one another while the chip carrier is in existence as an element separate from a chip to which the carrier may be attached in a later stage of manufacture. Stated another way, a coherent, self-supporting chip carrier is an element which can retain its structure and configuration prior to attachment to a chip or other structure. A coherent, self-supporting chip carrier is distinguished, for example, from a structure which is built up upon the surface of a chip, for example by applying a succession of coatings on the chip surface.

[0039] In a further process step, the chip carrier is then assembled with a chip 60 (FIG. 4) having a front face 62 with electrical contacts 64 thereon and having an oppositely facing rear face 66. In the particular embodiment illustrated in FIG. 4, the chip is disposed over the inner surface 24 of the dielectric layer and the front face 62 of the chip faces downwardly toward the inner face of the dielectric layer. As further explained below, other arrangements can be employed. The leads 36 are bonded to the contacts 64 on the chip as, for example, by forcing the leads into engagement with the contacts using a sonic bonding tool in a process which also breaks the frangible elements 44 (FIG. 1) and disconnects the leads from the anchors. During the lead-bonding process, the

chip 60 is spaced slightly from the dielectric layer and metallic layer of the chip carrier. For example, the plurality of small dielectric supports or "nubbins" 68 may be interposed between the front face of the chip and the chip carrier. Alternatively, one or a few preformed pads of a die attach material as discussed below in connection with FIG. 9 may be positioned on the chip or on the chip carrier, or fabricated as part of the chip carrier, so that the pad or pads covers a substantial portion or all of the chip surface and supports the chip above the chip carrier. In a further arrangement, a unitary pad or pads of die attach material can be made from a flowable die attach material applied to the surface of the chip or to the chip carrier prior to engaging the chip with the chip carrier.

[0040] After lead bonding, bond windows 28 are closed by a cover layer 70 which may be a very thin dielectric layer of the type commonly employed as a solder mask. Cover layer 70 may be provided over the entire outer surface 26 of the dielectric layer or, alternatively, may be provided only over the bond windows. Following application of the cover layer, an encapsulant 72 is introduced into the space between the chip and the dielectric layer and around the nubbins so as to form a composite spacer layer 73 including the encapsulant 72 and the nubbins 68. The encapsulant and the nubbins optionally may be formed from relatively soft materials as, for example, gels, elastomers, epoxies or other polymers, or from relatively rigid materials, or from a combination of relatively soft and relatively rigid materials. In the embodiment where the nubbins 68 are replaced by a larger pad or pads of die attach material, the pad or pads forms a part or all of the spacer layer 73. The cover layer 70 serves to prevent leakage of the encapsulant through the bond windows 28 during this process. The bumps 52 effectively seal the bump openings 30. Encapsulation processes of this general nature

are described in U.S. Patents 5,766,987; 5,659,952; 6,130,116 and 6,329,224, the disclosures of which are hereby incorporated by reference herein. In the embodiment illustrated, the cover layer 70 is left in place as a part of the finished product. In this embodiment, the cover layer effectively merges with dielectric layer 22 and forms a part of the dielectric layer in the finished article. In a variant of this process, the cover layer is removed after the encapsulant is injected and cured.

[0041] The resulting packaged semiconductor chip has self-supporting, generally cup-shaped bumps 52 electrically connected to the contacts 64 of the chip. Bumps 52 project downwardly (in the direction towards the bottom of drawing as seen in FIG. 4) and outwardly beyond the outer surface 26 of the dielectric layer (and beyond the cover layer 70). The encapsulant 72 which forms a portion of the supporting layer may also fill the interiors of cup-shaped bumps 52. Each bump 52 defines a rounded, convex bottom end 74 remote from the dielectric layer and chip at its bottom extremity. As seen in greater detail in FIG. 7, the exterior surface of the bottom end of the bump slopes upwardly in the direction outwardly away from the center of the bottom surface. Stated another way, a line 75 tangent to the exterior surface of the bump at a point slopes upwardly in the direction outwardly away from a vertical axis 77 extending through the bottom-most extremity of the bump. Desirably, this property is true for at least those points on the surface of the bump near the periphery of the bump, i.e., remote from axis 77, and positioned below the bottom surface 26 of the dielectric layer. The bump thus defines a sloping lead-in surface around the periphery of the bump and adjacent the bottom end of the bump. The exterior surface of the bump may be in the form of a surface of revolution about axis 77, and the bottom extremity of the bump may be in the form of a sphere or a sector of a sphere. In

this embodiment, the exterior surface of bump 52 is a continuous surface entirely encircling axis 77 from the bottom extremity of the bump to the outer surface 26 of the dielectric layer, with no holes or openings to the interior of the bump below the outer surface of the dielectric layer. Further, the bump is connected to the dielectric layer around the entire circumference of the bump, on all sides of axis 77.

[0042] If the foregoing steps are performed using a chip carrier or substrate large enough to accommodate numerous chips, the individual packages can be separated by severing the dielectric layer at this stage of the process or after the testing phase discussed below.

[0043] In the next phase of the process, the packaged chips are tested by engaging them with a test fixture 80 having electrically conductive elements 82 exposed at the top surface of the fixture. The conductive elements may incorporate openings 84 of the type commonly employed in sockets for receiving solder balls. Examples of such sockets are disclosed in U.S. Patents 5,802,699; 5,980,270; and 6,086,386, the disclosures of which are incorporated by reference herein. By way of example, the socket conductive elements 82 may include elements such as prongs or ridges (not shown) extending into or over openings 84 for providing high contact pressure at localized areas. Because the bumps 52 project downwardly below the dielectric layer, the bumps can be engaged in such openings in substantially the same way as solder balls. During the testing process, the packaged chip can be forced downwardly into engagement with the socket as, for example, by engaging the top surface of the packaged chip with a platen 86 and squeezing the packaged chip between the platen and the test fixture 82. During the testing procedure, the packaged chip is electrically tested by transmitting power, signals or both to the chip through bumps 52 and through the associated leads. The sloping lead-in surfaces on

the bumps facilitate engagement of the bumps with the openings 84 of the test fixture, and also wipe the edges of the openings and related features during engagement.

[0044] In the testing process, the bottom ends 74 of the individual bumps 52 desirably can be displaced independently of one another in the vertical direction upwardly and downwardly, toward and away from the chip 60. Although the present invention is not limited by any theory of operation, it is believed that the vertical displaceability of the bottom ends can be provided by deformation of the individual bumps 52 such as flattening of the convex bottom ends 74; by more generalized deformation of the bumps; by localized deformation of the dielectric layer 22; by localized deformation of spacer layer 73 to provide vertical movement of the entire bump or to allow tilting of individual bumps as, for example in the directions indicated by arrow 102; or by some combination of these factors. The relative importance of each of these factors will vary with the particular structure. However, regardless of the mechanism by which vertical displaceability is provided, vertical displaceability of the bump bottom ends facilitates reliable engagement of the bumps with the conductive elements 82 of socket or test fixture 80, even where the bump bottom ends 74, socket conductive elements 82 or both are slightly out-of-plane. Because the bump bottom ends can be displaced, reliable engagement can be achieved even where conductive elements 82 of the socket or test fixture 80 are fixed, relatively rigid structures. A test fixture with fixed, rigid conductive elements can be simple and relatively inexpensive. However, a test fixture with resilient conductive elements can be used if desired.

[0045] Moreover, the bumps can be engaged with contacts on the test fixture which are substantially planar and which do not incorporate the openings 84 in the contacts discussed above with reference to FIG. 5. For example, the contacts may

be flat structures similar to the contact pads 92 of the circuit panel discussed below. Here again, although the present invention is not limited by any theory of operation, it is believed that vertical displaceability of the bump bottom ends, the ability of the bumps 52 to tilt, and localized deformation of the bump bottom ends contribute to the ability of the bumps to make reliable contact with a planar contact pad. Thus, it is believed that some or all of these factors may provide "wipe" or relative movement between the surface of the bump and the surface of the contact pad.

[0046] After testing, the packaged chip can be mounted on a circuit panel 90 having pads 92 exposed at a top surface of the panel. As best seen in FIGS. 6 and 7, the circuit panel has a solder mask layer 94 overlying the top surface and apertures 96 in the solder mask layer, the pads being exposed through the apertures in this solder mask layer. The circuit panel also has traces 98 connected to the pads. The traces may extend within the circuit panel or on either side thereof and may be provided in any pattern.

[0047] The bottom ends 74 of the bumps 52 are bonded to contact pads 92 by a thin layer of a solder or other fusible electrically conductive bonding material. The bonding material or solder wets the metal of the bump 52 as well as the metal of the contact pad. Thus, the solder or other bonding material 100 forms a fillet extending up the exterior of the bump around the entire periphery of the bump. Depending upon the amount of bonding material present at each joint, the wetting properties of the bonding material and the height of bumps 52, the fillet may extend all the way to the outer surface 26 of the dielectric layer 22 or to the outer surface 71 of solder mask layer 70, which effectively forms a part of the outer surface 26 of the dielectric layer. The minimum thickness t of the bonding material layer at the lowermost extremities 74 of the bumps may be quite small or

even zero. That is, the convex, dome-shaped bump may touch the contact pad 92 at one or more points. Most preferably, the minimum bonding material layer thickness t is less than 50 microns and preferably less than 25 microns. Thus, the bonding material in the joints can have a thickness comparable to those commonly referred to as a "land grid array."

[0048] As discussed above, the bottom ends of the individual bumps can be displaced slightly upwardly and downwardly, towards and away from the chip independently of one another and can be flattened slightly by applied vertical forces. Thus, the bottom ends 74 of all of the bumps can be brought into engagement with the contact pads 92 by urging the packaged chip towards the circuit panel during bonding, even if the bottom ends of the bumps, the contact pads, or both, are slightly out of plane. Also, the sloping lead-in surfaces on the bumps can help guide the bumps into the apertures 96 in the solder mask layer. A similar action can be provided during engagement with a test fixture having a similar apertured layer.

[0049] The solder or other bonding material can be applied to the bumps themselves, or to the contact pads on the circuit panel, using techniques similar to those used in conventional surface-mounting of electronic components. Conventional fluxes may be used. Alternatively, conventional flux-less bonding techniques can be used. When the solder or other bonding material is brought to a liquid state and wets the bumps and contact pads, surface tension of the solder tends to draw each bump towards the center of the associated contact pad.

[0050] In the finished assembly, the solder joints provide good resistance to stresses resulting from differential thermal expansion of the components during service and during manufacture. Differences in expansion between chip 46 and circuit panel 90 tend to move contact pads 92 relative to the

contacts 64 on the chip. The bottom ends of the bumps can move relative to the chip. Some moveability is imparted by flexure of the bumps themselves. Also, although the present invention is not limited by any theory of operation, it is believed that the bumps can tilt to some degree, as, for example, in the directions indicated by arrow 102 in FIG. 6, as well as bend. Tilting of the bumps may be accompanied by local deformation of dielectric layer 22 and by deformation of the composite supporting layer provided by encapsulant 72 and nubbins 68. Even though there is only a very thin layer of solder present, the bumps provide strain relief action similar to that achieved by conventional solder balls having a height equal to the height of the bumps. Stated another way, the soldered bumps provide strain relief comparable to that of a ball grid array with the small solder volume found in a land grid array. The small solder volume minimizes environmental effects of the solder when the assembly is ultimately disposed of. For example, even where the solder contains a significant proportion of lead, reducing the volume of solder in the assembly reduces lead contamination of the environment. Still further reductions can be achieved by the use of solder with a relatively low proportion of lead.

[0051] In a further variant, the solder can be replaced by other bonding materials. For example, conductive polymer compositions such as metal-loaded polymers as, for example, silver-filled epoxies, can be used instead of solders. In a further variant, a layer of an anisotropic bonding material (not shown) may be provided over the contact pads 92 of the circuit panel and the bumps may be engaged with the contact pads, so that there is a thin layer of anisotropic bonding material between at least a part of the bottom end of each bump and the adjacent contact pads. Anisotropic bonding materials conduct in the direction through the layer but do not substantially conduct in the directions along the layer.

Typically, such materials include particles of conductive material dispersed in a dielectric material. Additional strain relief can be provided by flexing of leads 36 and deformation of the supporting layer and dielectric layer in areas remote from bumps.

[0052] The packaged chip 104 shown in FIG. 8 is similar to the packaged chip discussed above. Packaged chip 104 incorporates a chip carrier having a dielectric layer 122 with traces 138 and downwardly protruding bumps 154 integral with the traces. However, the traces and bumps are disposed on the outer surface 126 of the dielectric layer rather than the inner surface 124. Also, traces 138 are formed integrally with bonding pads 136 facing downwardly or outwardly on the outer surface 126 of the dielectric layer adjacent to a central bond window 128 extending through the dielectric layer. The chip 160 is disposed in a front-face down orientation, with contacts 164 disposed adjacent the center of the chip front surface 162 aligned with the bond window. The chip is secured to the inner surface 124 of the dielectric layer by a thin supporting layer of die attach material such an epoxy 168. The contacts 164 are connected to bond pads 136 by bonding wires 137 applied by a conventional wire bonding process. An encapsulant 172 covers the bond window 128 and bonding wires 137. A solder mask layer 170 covers the traces 138 but terminates short of bonding pads 136. The bumps 154 project downwardly through the solder mask layer. As is apparent from FIG. 8, the downward projection of bumps 154 from the dielectric layer is greater than the projection of the bonding wires 137 and encapsulant 172, so that the bumps can be bonded to pads 192 on a circuit panel 190 and engaged with a test fixture (not shown) without interference by the bonding wires and encapsulant.

[0053] Bumps 154 are similar to those discussed above. However, in forming bumps 154, the punch is engaged with the

inner surface 124 of the dielectric layer so that the dielectric layer as well as the metallic layer is deformed during the bump formation process, leaving a dielectric liner within each bump. Alternatively, holes can be provided in the dielectric layer above the bump-forming elements of the metallic layer and the punch can be advanced into engagement with the metallic layer through these holes.

[0054] In a further variant (FIG. 19) the metal layer 832, dielectric layer 822 and a layer 802 of a die attach material are provided as a laminate and engaged by a punch 846 so that all of these layers are deformed by the projections 848 on the punch. The deformed portions of the dielectric layer 822 and die attach layer 802 may remain in the positions indicated in FIG. 19, within the interior of the bumps 852. Alternatively, depending upon the resilience of these materials, one or both of the dielectric and die attach layers may spring back partially or completely to the flat condition as shown at 822' and 802' in FIG. 20, leaving hollow, unfilled bumps 852'.

[0055] The packaged chip depicted in FIG. 9 has traces 238 on the inner or upper surface 224 of the dielectric layer with bumps 254 similar to the bumps discussed above with reference to FIGS. 1-7, projecting through holes in the dielectric layer and formed integrally with the traces 238. Upwardly facing bonding pads 236 are also formed integrally with traces. The traces associated with bond pads 254a and 254b adjacent the center of the package are not illustrated; these traces also extend to bond pads disposed adjacent the edge of the dielectric layer. A composite spacer layer including a solder mask layer 270 and a layer of a die attach 272 separates the bumps and traces from the chip 260. The chip is mounted in face-up orientation overlying the inner surface 224 of the dielectric layer, with the front face 262 and contacts 264 facing upwardly, away from the dielectric layer and with the rear face 266 of the chip facing downwardly toward the

dielectric layer. Here again, the contacts 264 on the chip are connected to the bond pads by wire bonds 237. An overmolding 205 such as a relatively rigid epoxy overmolding covers the chip and the upper surface of the supporting layer. Packaged chips of this type can be handled and mounted in the same manner as discussed above.

[0056] As seen in fragmentary view in FIG. 10, a bump 354 may be formed as a generally U-shaped structure with a closed end defining the base of the U-shape and with a pair of upwardly extending legs 375 defining the open end 377 of the U-shape. One or both of the legs joins with a trace 338 formed integrally with the bump. A leg which does not join a trace may be joined with an anchor 339 which is electrically nonfunctional but which also serves to anchor the bump to the dielectric layer. Bumps of this type can be used in place of the generally cup-shaped bumps discussed above. The bump is mechanically connected to the dielectric layer at trace 338 and at anchor 339, and hence is mechanically connected to the dielectric layer at two or more points on opposite sides of the vertical axis 397 extending through the bottom extremity 374 of the bump. Other bump shapes can be employed, as, for example, a bump having a generally cruciform shape formed by two U-shapes extending in orthogonal planes and crossing one another at the bottom of the bump. Such a bump is mechanically connected to the dielectric layer at four points spaced around the vertical axis through the bottom end of the bump. In a further embodiment (FIG. 11), a bump 454 may be formed as a single projection with a single downwardly extending leg terminating with a bottom part 474 at a level lower than the level of the corresponding trace 438. The bottom part 474 is solder-bonded to a contact pad on the circuit panel in the same manner. Such a bump is connected to the dielectric layer 422 on only one side of the vertical axis 497 through the bottom extremity 474 of the bump as, for

example, at trace 438. For a given bump height and metal thickness, a bump connected in this manner typically will be more flexible than a closed bump such as that discussed above with reference to FIGS. 1-7 or a bump connected at multiple points such as the U-shaped bump of FIG. 10.

[0057] An assembly shown in FIGS. 12 and 13 includes a plurality of units 504 in a stacked arrangement. Each unit 504 includes a chip carrier having a dielectric layer 522 and bumps 554 formed integrally with the traces projecting downwardly from the traces and downwardly from the dielectric layer, the bumps extending through bump openings 530 in the dielectric layer. In this arrangement, however, chip 560 is mounted on the outer side 526 of the dielectric layer and connected by leads 526 interior with the traces (FIG. 12) extending through a bond window 528 in the dielectric layer to the contacts on the chip or by wire bonds (not shown). Bumps 554 are generally cup-shaped and similar to the bumps discussed above with reference to FIGS. 1-7. However, the bumps 554 of each unit project downwardly beyond the dielectric layer 522 and downwardly beyond the chip 560 so that the lowermost unit (the unit at the bottom in FIGS. 12 and 13) can be mounted on a circuit panel 590 and the bumps can be bonded to contact pads 592 in the same manner as discussed above with reference to FIGS. 1-7. Each unit 504 has a solder mask layer 570 overlying the traces 538 of the unit.

[0058] The solder mask layer has openings 539 aligned with the bumps, leaving the open top ends 555 of the bumps exposed at the top surface of the unit. The units desirably are substantially identical to one another, with their bumps disposed in the same manner and locations. Thus, the units can be stacked on one another as illustrated in FIGS. 12 and 13. The bottom ends 574 of bumps 554 on the second unit 504b are received in the open top ends 555 of the bumps 554 in the

first or lowermost unit 504a. Similarly, the bumps of unit 504c are received in the open top ends of the bumps in unit 504b and the bumps in the top unit 504d are received in the open top ends of the bumps in unit 504c. Any number of units can be stacked in this manner. The stacked units can be solder bonded as by solder 506. Also, each unit can serve as a test socket for the next higher unit. For example, the assembly of circuit panel 590 and bottom unit 504a can be used as a test socket for unit 504b or for another device having a similar bump layout. The closed bottom ends of the bumps in the unit under test make good contact with the interiors of the open top ends 555 of the bumps on the test socket. If the test is successful, the units can be separated from one another and solder can be introduced to bond the units to one another. Alternatively, an assembly of a circuit panel and a chip carrier, such as the chip carrier of unit 504a, can be used as a permanent test socket for testing other devices. The overall layout of the stacked assembly can be generally as described in co-pending, commonly assigned PCT International Application No. PCT/US02/32251, the disclosure of which is also incorporated by reference herein. As discussed therein, the conductive elements of stacked units form vertical busses. In assemblies as shown in FIGS. 12 and 13, the vertical busses are formed by stacked, interconnected bumps 554. As further discussed in the '351 international application, all of the units can be substantially identical to one another except that selective interconnection is provided between the vertical busses and chip select contacts on the chip within each unit. Typically, different units have chip select contact connected to different busses.

[0059] In a variant of the unit construction shown in FIG. 12, the chip can be disposed beneath the dielectric layer with the rear surface of the chip facing upwardly toward the outer surface of the dielectric layer. In yet another

variant, a stacked structure can be made with individual units each having a chip overlying the inner or upwardly-facing surface of the dielectric layer. In such a structure, the bumps on each unit extend downwardly past the chip on the next lower unit. The structure of each unit may be similar to the packaged chips shown in FIGS. 1-9, except that some or all of the bumps are disposed outside the periphery of the chip so that the bumps on the stacked units can be engaged with one another.

[0060] A test socket according to yet another embodiment of the invention includes a substrate 690 such as a circuit panel and a flexible dielectric element 622 having bumps 654 projecting downwardly therefrom, the bumps being formed integrally with traces 638 on the dielectric element. The traces terminate in socket openings 639. The bumps 654 support the dielectric element 622 above the substrate 690 and electrically interconnect the test sockets 639 with the contact pads 692 of the substrate and with leads (not shown) in the substrate. Desirably, the bumps 654 are provided in a grid pattern as are the socket openings 639. The grid of socket openings 639 is interspersed with the grid of bumps 654 so that each socket opening 639 is surrounded by a plurality of bumps 654. The bumps 654 serve as supporting posts and perform the functions of the supporting posts as described in U.S. Patent 6,086,386, the disclosure of which is hereby incorporated by reference herein. The test socket can be used to test a microelectronic unit 604 having projecting elements 606 which may be bumps, solder balls or other projecting elements. In the manner described in the '386 patent, when a unit 604 being tested is pressed downwardly into engagement with the test socket, the projections 606 on the unit engage the socket opening 639 and thence are electrically connected to traces 638 and bumps 654 and thence connected to the substrate. The dielectric element 622 and traces 638 can

deform as indicated in broken line 622´ and 638´. This action is similar to the action of the flexible socket discussed in the '386 patent. However, the use of bumps formed integrally with traces 638 greatly simplifies construction of the socket. Alternatively, the open ends 655 of the bumps can be employed as openings for receiving the projections of the unit under test as discussed above with reference to FIGS. 12 and 13.

[0061] Numerous variations and combinations of the features discussed above can be utilized without departing from the present invention. For example, more than one chip can be mounted on a chip carrier. Multiple chips can be mounted on opposite sides of the chip carrier, stacked on one side of the chip carrier or arrayed on one or both sides so that chips are disposed side by side. In a further arrangement, bumps may be used in place of terminal pads and solder balls in a folded chip carrier or assembly as discussed in U.S. Patent 6,121,676 and in commonly assigned, co-pending U.S. Provisional Application Serial Nos. 60/401,391 and 60/403,939, the disclosures of which are also incorporated by reference herein.

[0062] In yet another arrangement, a metal layer such as a continuous sheet of metal can be deformed to form the bumps before the metal layer is united with the dielectric layer as, for example, engaging the metal layer between a punch and die as discussed above. The metal layer can then be etched using a conventional photoresist as an etch mask to form traces and other features such as bonding pads and leads. In a further variant, the process of forming the bumps may be integrated with a process of forming the traces and other features of the type shown in U.S. Patent 6,083,837, the disclosure of which is hereby incorporated by reference herein. A layer of metal 702 having substantially uniform thickness (FIG. 15) is engaged between tools such as 750 and 754 (FIG. 16) to form bumps 752 and also to form relatively thick regions 704 in

areas where traces, leads and other features are to be formed and relatively thin regions 706 in other parts of the sheet. Following this deformation or "coining" process, the metal layer is united with a dielectric layer 722 (FIG. 17) and then etched for a time sufficient to completely remove the metal in thin regions 706 but insufficient to completely remove the metal in the thick regions 704 and bumps 752. This leaves the bumps 752, traces 738 and other metallic features 708. The dielectric layer may overlie either side of the metal layer, and may be applied either as a pre-formed dielectric layer or as a coating on the metal layer which is cured to form a coherent dielectric layer prior to etching the metal. In a further variant, coining step used to form the thin and thick regions of the metal layer may be performed in a separate operation from the deforming step used to make the bumps. In the embodiment of FIGS. 15-17, the die 754 (FIG. 16) has cavities which are in the form of the desired bump shape, so that at least the bottom end of the bump is formed by contact with the die. Such a die can be used in the other embodiments discussed herein. Also, the die can be provided with one or more small indentations or grooves to form raised features such as a microscopic projection 757 on the bottom end of the bump or raised ridges (not shown) extending along the bottom or side walls of the bump. Such raised features may have sharp corners or edges, and facilitate good contact with test fixtures and/or contact pads.

[0063] In a further variant, processes such as electroplating can be employed to form the bumps. For example, the metallic layer can be formed with bumps by electroplating it on a male mandrel having projections corresponding to the bumps to be formed or on a female mold having recesses corresponding to the bumps to be formed. Where the bumps are formed by mechanical deformation, a punch with projections as discussed with reference to FIG. 3 can be used

with a cushion of a relatively hard, resilient material in place of the die. Also, regardless of the method used to form the bumps, the bumps may be solid, metal-filled structures such as the bump 952 depicted in FIG. 21. Bumps of this type can be formed without indenting the top of the metallic layer, and accordingly can be formed by a die having cavities in the desired bump shape opposed by a flat tool. Bump 952 has a bottom extremity 974 which is flat and horizontal in the immediate vicinity of the central vertical axis 977, but which also has a sloping or curved edge surface 902 defining the margins of the bottom extremity, remote from the axis. This sloping or curved edge surface 902 provides a lead-in similar to the lead-in provided by the curved bottom surface 74 of the bump discussed above with reference to FIGS. 1-7. In a further variant, the flat bottom extremity may extend all the way to the edges of the bump, where it joins with the vertically-extensive wall of the bump. Flat bottom extremities can be provided on hollow bumps as well as on solid bumps. The flat bottom extremity of the bump further minimizes the amount of solder or other bonding material needed to join the bottom extremity to a contact pad of a circuit panel.

[0064] In a further variant (FIG. 22), the bump 1052 projects downwardly from a trace 1038, but does not project beyond the bottom surface 1026 of dielectric layer 1022. Although the bumps are recessed from bottom surface 1026 within openings 1030, they are nonetheless exposed at the bottom surface and hence accessible for connection from the bottom surface. As used in this disclosure, a metallic feature can be considered "exposed at" a surface of a dielectric layer if the metallic feature is accessible to a contact or bonding material applied to such surface. Thus, a metallic feature which projects from the surface of the dielectric (such as the bumps 52 of FIGS. 1-7) or which is

flush with the surface of the dielectric is also "exposed at" such surface.

[0065] When the packaged chip of FIG. 22 is attached to a circuit panel, solder or other bonding material 1010 extends upwardly from pad 1092 to the bottom end 1074 of the bump, and bonds to the bump within the bump opening 1030 of the dielectric layer. Here again, the quantity of bonding material required to form the joint is substantially less than that which would be required with flat pads at the top surface 1024. The dielectric layer may constrain the bonding material during bonding and thus further limit the volume of bonding material required. Also, the downwardly-projecting bumps in this embodiment as well tend to minimize stress on the bonding material.

[0066] As these and other variations and combinations of the features discussed above can be utilized without departing from the present invention as defined by the claims, the foregoing description of the preferred embodiment should be taken by way of illustration rather than by way of limitation of the invention.